REMARKS

Filed concurrently herewith is a Request for a One Months Extension of Time which extends the shortened statutory period for response to September 2, 2005. Accordingly, it is respectfully submitted that this response is being timely filed.

The Official Action dated May 2, 2005 has been received and its contents carefully noted. In view thereof, claims 1-3, 13, 15 and 16 have been canceled in their entirety without prejudice nor disclaimer of the subject matter set forth therein, claims 4, 6, and 9-12 have been amended and new claims 20-22 have been added in order to better define that which Applicants regard as the invention. Accordingly, claims 412, 14 and 17-22 are presently pending in the instant application with claims 17-19 being withdrawn from further consideration by the Examiner as being directed to a non-elected invention.

With reference now to page 2 of the Office Action, claims 1-5 and 11-16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,111,278 issued to Eichelberger in view of U.S. Patent No. 6,582,991 issued to Maeda and US Patent Publication 2002/0122244 to Sotgiu et al. This rejection is respectfully traversed in that the combination proposed by the Examiner neither discloses nor suggests that which is presently set forth by Applicant's claimed invention.

As can be seen from the foregoing amendments, each of independent claims 1, 15 and 16 have been canceled in favor of new independent claims 20, 21 and 22. It is noted that new independent claim 20 recites a passive element chip comprising a substrate, an insulating layer formed on the substrate, an inductor formed in the insulating layer by a first metal wire, a capacitor formed in the insulating layer by a second metal wire wherein the capacitor is isolated from the inductor, a protective film formed on the insulating layer with the protective film having a first opening for exposing the inductor and a second opening for exposing the capacitor, a first wiring pattern formed within the first opening and a second wiring pattern formed within the second opening. Similarly, independent claim 21 recites a passive element chip formed by being diced off from a wafer, comprising a substrate, an insulating layer formed on the substrate an inductor formed in the insulating layer by a first metal wire, a capacitor which is formed in the insulating layer by a second metal wire with a capacitor being isolated from the inductor, a protective film formed on the insulating layer wherein the protective film has a first opening for exposing the inductor and a second opening for exposing the capacitor, a first wiring pattern for connecting to an external source formed

within the first opening and a second wiring pattern for connecting to the other external source formed within the second opening.

Further, new independent claim 22 recites an integrated module comprising a first substrate, an insulating film formed on the first substrate, a passive element chip within the insulating film and being formed on the first substrate and a semiconductor chip within the insulating film and being formed on the first substrate wherein the passive element chip comprises a second substrate different from the first substrate, an insulating layer formed on the second substrate, an inductor formed in the insulating layer by a first metal wire, a capacitor formed in the insulating layer by a second metal wire with the capacitor being isolated from the inductor and a protective film formed on the insulating layer. It is respectfully submitted that the combination proposed by the Examiner clearly fails to disclose or remotely suggest these features.

Particularly, it noted that U.S. Patent No. 5,111,278 issued to Eichelberger merely shows the IC chips 38 in figure 1 and referred to in column 8, line 55, the IC chips 74 in figure 5 and referred to in column 13, line 11 and the chips 106 in figures 7 referred to in column 16 line 15. Maeda et al. shows the electronic component 200 which is a capacitor, a resistor, as shown in figure 2 and referred to in column 13, lines 29-30. However, it is respectfully submitted that each of these cited references fail to disclose or remotely suggest an inductor which is formed in the insulating layer by a first metal wire, a capacitor which is formed in the insulating layer by a second metal wire wherein the capacitor is isolated from the inductor as is recited in new independent claim 20. Further, the references clearly fail to disclose or suggest an inductor which is formed in the insulating layer by a first metal wire, a capacitor which is formed in the insulating layer by a second metal wire wherein the capacitor is isolated from the inductor as recited in new independent claim 21 and further fails to disclose or suggest an inductor which is formed in the insulating layer by a first metal wire, a capacitor which is formed in the insulating layer by a second metal wire wherein the capacitor is isolated from the inductor as recited in new independent claim 22.

While the patent to Maeda et al. may show a stand alone electronic component 200 for example a chip resistor, this reference fails to disclose or remotely suggest the passive element having the inductor formed by a first metal wiring and the capacitor formed by a second metal wire wherein the capacitor and the inductor are isolated from one another. Accordingly, it is respectfully submitted that Applicants claimed invention has set forth in each of new independent claims 20, 21 and 22 as well as those claims which depend

therefrom clearly distinguishes over the combination proposed by the Examiner and are in proper condition for allowance.

It is further noted that the Examiner in rejecting Applicants claimed invention refers to U.S. Patent Publication No. 2002/0122244 as being Lin et al. However, it is noted that U.S. Patent Publication 2002/0122244 is in fact that of Sotgiu et al. and consequently Applicants remarks and amendment set forth hereinabove have been carried out in this manner. However, if the Examiner did not intend this to be the case, it is respectfully submitted that the Examiner clarify the rejection of claims 1-5 and 11-16 and afford Applicant the opportunity to properly respond to such clarified rejection.

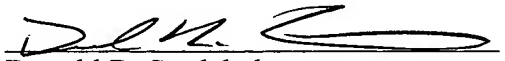
With reference now to Paragraph 4 of the Office Action, claims 6-10 have been rejected under 35 U.S.C. 103 (a) as being unpatentable over Eichelberger, Maeda et al. and Lin et al. has applied claim 1 above and further in view of U.S. Patent No. 6,853,559 issued to Panella et al. This rejection is likewise respectfully traversed that the patent to Panella et al. does nothing to overcome aforementioned shortcomings associated with the combination proposed by the Examiner.

That is, while Panella may show a system for an integrated circuit and particularly that illustrated in figure 1 thereof, it is respectfully submitted that this reference clearly fails to disclose remotely suggesting an inductor which is formed in the insulating layer by a first metal wire, a capacitor which is formed in the insulating layer by a second metal wire wherein the capacitor is isolated from the inductor as is recited in each of independent claims 20, 21 and 22 of Applicants claimed invention.

Therefore, in view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner that claims 4-12, 14 and 20-22 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



Donald R. Studebaker
Reg. No. 32,815
Nixon Peabody LLP
401 9th Street N.W.
Suite 900
Washington, D. C. 20004
(202) 585-8000